Progress towards a micromachined thermoelectric generator using PbTe and PbSnSeTe thin films

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Abstract

This paper presents etching techniques and metal contact resistance studies for vapor-deposited PbTe and PbSnSeTe films to enable micromachining of thermoelectric (TE) generators within integrated MEMS devices (e.g. micro heat engines, microcombustors). Films of up to 10 µm were achieved using (100) silicon substrates. Single-crystal films were achieved using CdTe or ZnTe buffer layers, while polycrystalline films were formed on thermally-oxidized silicon. Processes using a bromine-based wet etch and methane-based ICP plasma etch yielded etch rates of 3 µm/min and 0.65 µm/min, respectively, with high selectivities (>10:1) to photoresist, silicon and SiO_2. Electrical resistivity (van der Pauw) and metal contact resistance (transfer length method) test structures were used to characterize patterned PbTe and PbSnSeTe films and the contact resistance with a variety of metals (Au/Cr, Au, Pt, Ni, Cu, Pt). Film resistivities of 5-300 mΩ-cm and ohmic contacts with specific contact resistivities of 0.4-40 mΩ-cm² were achieved.

Keywords: contact resistance, lead telluride alloys, microfabrication, specific contact resistivity, thermoelectric generator

1 - INTRODUCTION

In recent years, improvements in thermoelectric (TE) material properties over a wide temperature range have spurred interest in microscale TE generators. As a result, designs have been proposed involving a variety of thin films such as poly-Si, poly-SiGe, V-VI, and IV-VI alloys [1-3]. The exploitation of TE microelectromechanical systems (MEMS) for power generation is attractive due to the possibility for silent, environmentally friendly, and low maintenance operation with no moving parts [4].

Theoretical and experimental studies have suggested using IV-VI materials such as PbTe alloys for TE generators [5-8]. In the past, IV-VI materials have also been used in heterojunction infrared detectors [9] and TE coolers [10], yet, little is reported regarding thin film microfabrication issues (deposition and etching) or metal-semiconductor contact resistances to these films. While the contact resistance is often negligible on the macroscale, it can become a limiting factor in the performance of microscale TE generators [11]. Moreover, understanding and characterizing relevant microfabrication issues is critical to future integration and deployment of thin film TE materials within micromachined silicon MEMS. Thus, the goal of this work is to characterize and enhance microfabrication methods to improve the performance and integration of microscale TE generators.

2 - EXPERIMENTAL PROCEDURE

2.1 - Material Deposition

Standard grade 3-inch (100) silicon wafers were used as starting substrates. PbTe and selected compositions of the $Pb_{(1-x)}Sn_xSe_yTe_{(1-y)}$ IV-VI pseudo-binary materials system were deposited onto buffer layers of CdTe, ZnTe, or thermally-grown SiO_2, which provided electrical insulation between the bulk silicon and the IV-VI TE materials. Both single-crystal (s.c.) and polycrystalline films were investigated. The polycrystalline films may offer a better thermoelectric figure or merit because of reduced thermal conductivity. However, while methods for achieving s.c. IV-VI films on silicon are well-developed at the U.S. Army Research Lab, integration of polycrystalline IV-VI films on silicon presented several new challenges, as described below.

The IV-VI films were vapor-deposited using congruent sublimation of the solid-source parent compounds, e.g. PbTe and SnSe, in UHV. The deposition rate was nominally 1 µm/hr for all films, and the substrate temperature was 300 °C. The base pressure for the system was generally 10^{-10} to 10^{-9} Torr. P-type impurity doping was achieved using an independent Tl_2Te source during deposition and was targeted to $10^{19}/cm^3$.

Deposition onto CdTe or ZnTe buffer layers yielded relatively defect-free s.c. surfaces, even for film thicknesses up to 10 µm (Fig. 1a,b). In contrast, deposition onto the thermally-grown SiO_2 buffer layers yielded polycrystalline films with film striations and cracks (Fig. 1c,d). These surface features appear to be consistent with mismatch between the thermal expansion coefficients of the IV-VI, SiO_2, and Si materials [12]. Improvements to the polycrystalline film deposition methods are ongoing.

2.2 - Etch Studies

Samples of PbSnSeTe (~ 5mm x 5mm) were ICP dry etched with a methane-based mixture in a Uniaxis Shuttleback RIE/ICP chamber. Various mixtures of methane, hydrogen,

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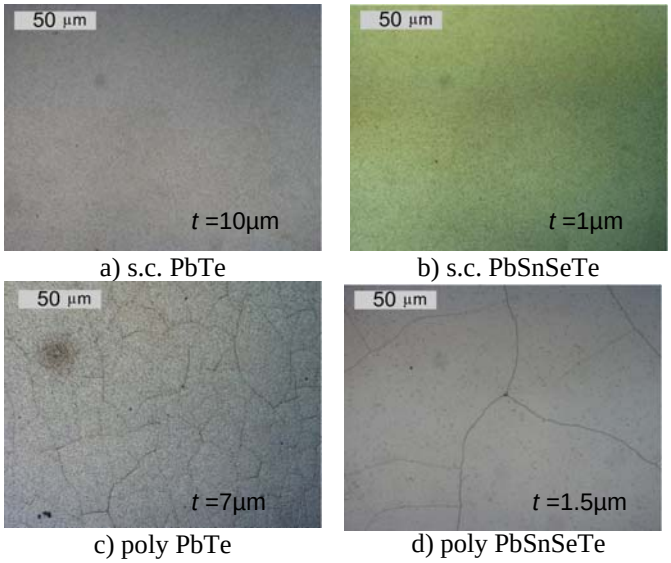


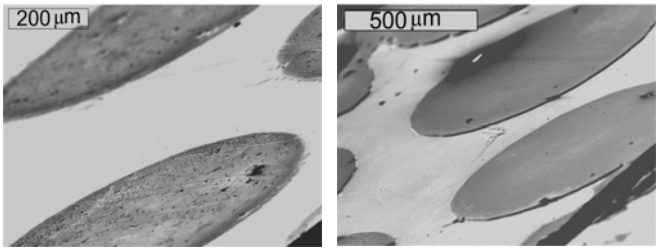
a) s.c. PbTe b) s.c. PbSnSeTe

c) poly PbTe d) poly PbSnSeTe

Figure 1 – Optical images of PbTe with various film thickness (s.c. = single crystalline, poly = polycrystalline).

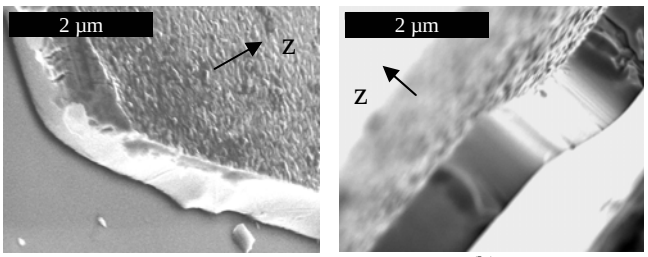
and argon were used to etch the alloy films [13] with 55 sccm total gas flow, 25 mTorr chamber pressure, and 600 W RF power (100 W DC bias), with backside cooling (10 sccm of He gas) (Fig. 2a.). An etch rate up to 0.65 µm/min was achieved for PbSnSeTe using 45:5:5 sccm of CH_4:H_2:Ar_2. Silicon test samples showed 200-300 nm etch for a 10 min. duration, indicating an etch selectivity to silicon >10:1. The plasma etch also showed good selectivity to photoresist (>10:1). During these tests, it was observed that the photoresist had become scorched when etched for an extended amount of time, typically more than 5 min. This burned masking layer was not easily removed in O_2 plasma using a barrel asher, leaving a residue on the PbTe alloys. This limited the effectiveness of the dry etching approach, especially for thicker films, where long etch times are required.

Due to issues with removing the residual masking layer and relatively slow etch rates, wet etch methods were also investigated. A variety of thin-film samples were wet etched using a bromine-based solution (Fig. 2b) [12,14]. This solution consisted of 20:20:1 (by volume) of H_2O:HBr:Br_2 at room temperature. The process yielded an etch rate ~ 3 µm/min for both s.c. and polycrystalline PbTe and PbSnSeTe films. Also, good selectivities to silicon (>10:1), PECVD SiO_2 (>10:1), and photoresist (>10:1) were observed. In summary, the wet etch yielded a faster etch rate (~ 5x) and a cleaner surface compared to the dry etch. However, mask undercut was observed in some of the wet etch samples, especially for long etch times. Scanning electron microscopy (SEM) images show the surface roughness and sidewall profile for these thin films (Fig. 3).



(a) (b)

Figure 2 – Comparison SEM images for patterned PbSnSeTe films using (a) methane-based ICP plasma etch and (b) bromine-based wet etch.



(a) (b)

Figure 3 – Topography SEM images of wet etched PbSnSeTe films. The z-vector indicates the direction normal to the wafer surface.

2.3 – Electrical Test Structure Fabrication

Electrical test structures [15] were fabricated using a combination of photolithography, wet etching, metal sputtering, and lift-off methods. Transfer length method (TLM) structures were used for contact resistance and resistivity measurements, and van der Pauw structures were used for supplementary resistivity measurements (Fig. 4c).

First, positive photoresist (Clariant AZ 9260) was spun on the wafer surface and soft-baked at 95 °C for 30 min. Photolithography was used to pattern the photoresist mask, and the bromine-based wet etch was used to define isolated PbTe film structures (Fig. 4a). Next, another photoresist layer was patterned to serve as a lift-off mask for the contact pad metallization. A variety of different metals (Au/Cr, Au, Pt, Ni, Cu, Pt) were deposited (~ 500nm) using an RF sputterer (chamber pressure at ~ 3.7 mTorr), or via evaporation. In the case of sputtering, an in-situ plasma cleaning, consisting of O_2 gas followed by brief argon sputtering (200 W), was performed to remove organic residues and any native oxide on the PbTe films. After metal deposition, a brief ultrasonic agitation in acetone was used to lift-off the metal layer (Fig. 4b,c). The completed test structures are shown in Fig. 5.

2.4 - Electrical Measurements

TLM Structures

Transfer length method (TLM) test structures can be used to evaluate contact resistance and resistivity parameters [14]. A series of well-defined metal contacts are patterned onto an

isolated mesa of PbTe. Assuming a non-alloyed metal-semiconductor interface, the total resistance, R_T, between two adjacent contacts is given as [15]:

$$R_T = \frac{\rho}{t \cdot z} d + \frac{2\rho_c}{A_c} \quad (1)$$

where ρ is the film resistivity, t is the film thickness, d is the spacing between adjacent contacts, z is the metal contact length, $\rho_c = R_c \cdot A_c$ is the specific contact resistivity (R_c is the contact resistance), and $A_c = z^2$ is the contact area (Fig. 4c).

This equation assumes (1) the contact length extends nearly to the edge of the mesa ($z \approx w$) to minimize current crowding effects, and (2) the contact length is greater than the transfer length ($z > 1.5L_t$), where $L_t = \sqrt{\rho_c \cdot t / \rho}$ [16].

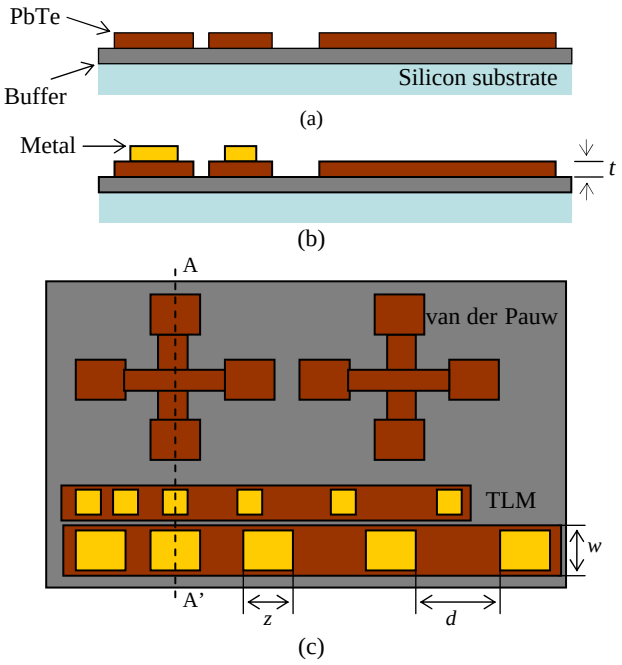


Figure 4 – Process for electrical test structures. (a) Electrically insulated PbTe film. (b) Contact metallization. (c) Top view of van der Pauw and TLM test structures.

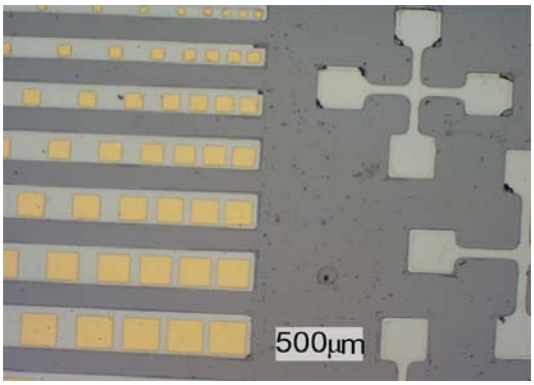


Figure 5 – Optical image of s.c. Au/Cr/PbTe patterned test structures.

A series of measurements between contacts with different spacing is used to generate a plot of R_T vs. d, as shown in Fig. 6. The contact resistance can be determined from the x-intercept (d = 0), and the semiconductor resistivity can be calculated from the slope of the curve. Four-point probe measurements were made using an HP4294A precision impedance analyzer and Keithley 2400 Sourcemeter. A linear I-V curve, using an Agilent 4155C semiconductor parameter analyzer, verified ohmic contacts to the films. The electrical contacts ranged from 225-400 µm in length. The results for various metals and film types are summarized in Table 1. Using TLM structures, the calculated contact resistivity to s.c. films was ρ_c = 0.62 ± 0.09 mΩ-cm² with film resistivity ρ = 5.29 ± 0.36 mΩ-cm (95% confidence interval). The transfer length L_t was 88.8 µm, indicating long contacts since z/L_t >1.5. Meanwhile, large deviations were found in contact resistivity to polycrystalline films.

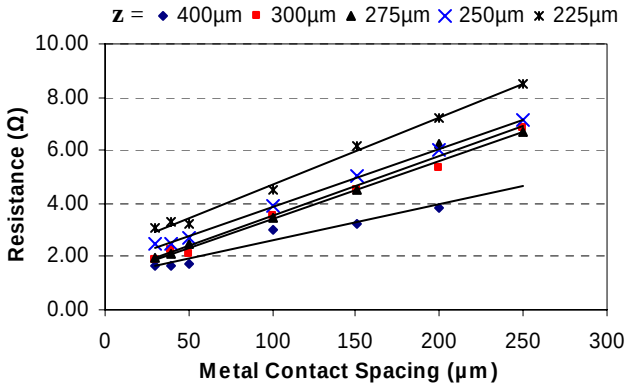


Figure 6 – Contact resistance characterization with Au/Cr ohmic contacts on s.c. PbTe films.

Van der Pauw Structures

To compliment the TLM tests, film resistivities were also obtained from the van der Pauw test structures [17]. For the case of thin film samples, i.e. films with thickness much less than probe spacing, the measured resistivity is given by:

$$\rho = \frac{\pi \cdot t}{\ln(2)} \frac{V}{I} \quad (2)$$

In this study, the film thicknesses are at most 10 µm and the probe spacing is > 250 µm, validating the thin film assumption. Using this method, film resistivities of 51.7 ± 36.9 mΩ-cm were measured for s.c. films, as depicted in Table 1.

3 – CONCLUSIONS

Numerous samples of thin film binary PbTe and quaternary PbSnSeTe alloys were successfully microfabricated on silicon wafers. This demonstrates the potential to integrate IV-VI thin films with varied starting substrate conditions (i.e. s.c. films on CdTe or ZnTe and polycrystalline films on SiO_2). Microfabrication methods have been developed to deposit, etch and pattern ohmic contacts to these films as a

Table 1 – Measurement and observations on PbTe films (sc = single crystalline, poly = polycrystalline) with RF sputtered metal contacts. Pt, Au, Cu, Ni (200nm). Au/Cr (500/50nm). Uncertainty bounds represent a 95% confidence interval.

Film	Type	Film thickness (μm)	Notes on films	Metal Contacts	ρ_c (mΩ-cm²) TLM	Film ρ (mΩ-cm) TLM	Film ρ (mΩ-cm) van der Pauw
PbTe	sc	9-10	Smooth surface	Au/Cr	0.62 ± 0.09	5.29 ± 0.36	51.7 ± 36.9
	poly	7	Severe cracks	Pt Au Cu Ni	0.44 ± 4.9 2.4 ± 9.1 6.2 ± 19.6 41.6 ± 13.9	168 ± 23	302 ± 300
PbSnSeTe	sc	0.7-1.2	Smooth, some striations	-	-	-	-
	poly	1.5	Striations (minor cracks)	Pt (100nm) (evaporated)	16.3 ± 38.1	324 ± 121.3	208 ± 202

step toward the development of a micromachined PbTe-based TE generator. Overall, s.c. films showed a smooth surface and some striations; while polycrystalline films (on oxide) indicated severe cracks on thicker samples and some striations on thin samples. Because of these defects, electrical resistivity and contact resistance measurements on the polycrystalline films were severely compromised, due to large measurement uncertainties. However, the data seems to indicate that that s.c. films have lower contact resistance and resistivity compared to the polycrystalline films. Better film surfaces are needed to obtain more definitive measurements.

Recent improvements in film deposition techniques have yielded defect-free polycrystalline surfaces. Ongoing work will include characterization of these films and contact metallurgies. Efforts will also be directed to reduce the polycrystalline contact resistance, possibly by hydrogen forming gas annealing. The material properties may also be evaluated as functions of temperature.

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